CLAIMS:

1. A method of depositing an aluminum nitride comprising layer over a semiconductor substrate comprising:

positioning a semiconductor substrate within a chemical vapor deposition reactor; and

feeding ammonia and at least one compound of the formula R_3Al, where "R" is an alkyl group or a mixture of alkyl groups, to the reactor while the substrate is at a temperature of about 500°C or less and at a reactor pressure from about 100 mTorr to about 725 Torr effective to deposit a layer comprising aluminum nitride over the substrate at such temperature and reactor pressure.

2. The method of claim 1 wherein substrate temperature and reactor pressure are maintained substantially constant during the feeding and deposit.

3. The method of claim 1 wherein substrate temperature is greater than or equal to about 250°C during the feeding.

4. The method of claim 1 wherein substrate temperature is from about 380°C to about 420°C during the feeding.

5. The method of claim 1 wherein the aluminum nitride is substantially amorphous.

6. The method of claim 1 wherein the reactor is void of plasma during the depositing.

7. The method of claim 1 wherein the compound comprises triethylaluminum.

8. The method of claim 1 wherein the compound comprises trimethylaluminum.

9. The method of claim 1 wherein the compound comprises at least two different alkyl groups.

10. The method of claim 1 wherein the compound comprises at least one methyl group and at least one ethyl group.

11. A method of forming DRAM circuitry comprising:

forming a first capacitor electrode over a substrate;

feeding ammonia and at least one compound of the formula R_3Al, where "R" is an alkyl group or a mixture of alkyl groups, to a chemical vapor deposition reactor within which the substrate is received while at a temperature of about 500°C or less and at a reactor pressure from about 100 mTorr to about 725 Torr effective to deposit a capacitor dielectric layer comprising aluminum nitride over the first capacitor electrode;

forming a second capacitor electrode over the aluminum nitride comprising capacitor dielectric layer; and

providing a DRAM word line comprising a gate of a field effect transistor which has a pair of source/drain regions, one of the source/drain regions being provided in electrical connection with the first capacitor electrode, the other of the source drain regions being provided in electrical connection with a DRAM bit line.

12. The method of claim 11 wherein the compound comprises triethylaluminum.

13. The method of claim 11 wherein the compound comprises trimethylaluminum.

14. The method of claim 11 wherein the compound comprises at least two different alkyl groups.

15. The method of claim 11 wherein the compound comprises at least one methyl group and at least one ethyl group.

16. The method of claim 11 wherein substrate temperature is greater than or equal to about 250°C during the feeding.

17. The method of claim 11 wherein substrate temperature is from about 380°C to about 420°C during the feeding.

18. The method of claim 11 wherein substrate temperature and reactor pressure are maintained substantially constant during the feeding and deposit.

19. The method of claim 11 wherein the aluminum nitride is substantially amorphous.

20. The method of claim 11 wherein the reactor is void of plasma during the depositing.

21. DRAM circuitry comprising:

an array of word lines forming gates of field effect transistors and an array of bit lines, individual field effect transistors comprising a pair of source/drain regions; and

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a plurality of memory cell storage capacitors associated with the field effect transistors, individual storage capacitors comprising a first capacitor electrode in electrical connection with one of a pair of source/drain regions of one of the field effect transistors and a second capacitor electrode, a capacitor dielectric region received intermediate the first and second capacitor electrodes, the region comprising aluminum nitride, the other of the pair of source/drain regions of the one field effect transistor being in electrical connection with one of the bit lines.

22. The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of aluminum nitride.

23. The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes.

24. The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 60 Angstroms.

25. The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 50 Angstroms.

26. The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of aluminum nitride, and has a thickness less than or equal to 60 Angstroms.

27. The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 60 Angstroms.

28. The circuitry of claim 21 wherein the aluminum nitride is substantially amorphous.

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29. A method of forming a field emission device comprising:

forming an electron emission substrate comprising emitters;

providing the emission substrate within a chemical vapor deposition reactor;

feeding ammonia and at least one compound of the formula R_3Al, where "R" is an alkyl group or a mixture of alkyl groups, to the reactor while the electron emission substrate is at a temperature of about 500°C or less and at a reactor pressure from about 100 mTorr to about 725 Torr effective to deposit a layer comprising aluminum nitride over at least a portion of the emitters; and

after the deposit, joining the electron emission substrate with an electron collector substrate.

30. The method of claim 29 wherein the electron collector substrate comprises a face plate comprising phosphor, and comprising forming the device to comprise a field emission display.

31. The method of claim 29 wherein the electron emission substrate comprises a conductive extraction grid formed outwardly of and spaced from the emitters, the deposit occurring after formation of the extraction grid.

32. The method of claim 29 wherein the electron emission substrate comprises a conductive extraction grid formed outwardly of and spaced from the emitters, the deposit occurring after formation of the extraction grid and also occurring on the extraction grid.

33. The method of claim 29 wherein the compound comprises triethylaluminum.

34. The method of claim 29 wherein the compound comprises trimethylaluminum.

35. The method of claim 29 wherein the compound comprises at least two different alkyl groups.

36. The method of claim 29 wherein the compound comprises at least one methyl group and at least one ethyl group.

37. The method of claim 29 wherein electron emission substrate temperature is greater than or equal to about 250°C during the feeding.

38. The method of claim 29 wherein electron emission substrate temperature is from about 380°C to about 420°C during the feeding.

39. The method of claim 29 wherein electron emission substrate temperature and reactor pressure are maintained substantially constant during the feeding and deposit.

40. The method of claim 29 wherein the aluminum nitride is substantially amorphous.

41. The method of claim 29 wherein the reactor is void of plasma during the depositing.

42. A field emission device comprising:

an electron emitter substrate comprising emitters having at least a partial covering comprising aluminum nitride; and

an electrode collector substrate spaced from the electron emitter substrate.

43. The field emission device of claim 42 wherein the electron collector substrate comprises a face plate comprising phosphor, and the field emission device comprises a field emission display.

44. The field emission device of claim 42 wherein the electron emission substrate comprises a conductive extraction grid formed outwardly of and spaced from the emitters, the covering being received over the extraction grid.

45. The field emission device of claim 42 wherein the electron emission substrate comprises a conductive extraction grid formed outwardly of and spaced from the emitters, aluminum nitride of the covering being in contact with the extraction grid.

46. The field emission device of claim 42 wherein the emitter covering consists essentially of aluminum nitride.

47. The field emission device of claim 42 wherein the emitter covering is void of oxide.

48. The field emission device of claim 42 wherein the aluminum nitride is substantially amorphous.

49. The field emission device of claim 42 wherein the covering comprises a thickness less than or equal to about 150 Angstroms.

50. The field emission device of claim 42 wherein the covering comprises a thickness greater than or equal to about 50 Angstroms.

51. A field emission device comprising:

an electron emitter substrate comprising emitters having at least a partial covering comprising an electrically insulative material other than an oxide of silicon; and

an electrode collector substrate spaced from the electron emitter substrate.

52. The field emission device of claim 51 wherein the electron collector substrate comprises a face plate comprising phosphor, and the field emission device comprises a field emission display.

53. The field emission device of claim 51 wherein the electron emission substrate comprises a conductive extraction grid formed outwardly of and spaced from the emitters, the covering being received over the extraction grid.

54. The field emission device of claim 51 wherein the electron emission substrate comprises a conductive extraction grid formed outwardly of and spaced from the emitters, aluminum nitride of the covering being in contact with the extraction grid.

55. The field emission device of claim 51 wherein the covering comprises a thickness less than or equal to about 150 Angstroms.

~~56. The field emission device of claim 51 wherein the covering comprises a thickness greater than or equal to about 50 Angstroms.~~

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